CONTINUOUS, IN-LINE PROCESSING OF CdS/CdTe DEVICES: PROGRESS TOWARDS CONSISTENT STABILITY

R. A. Enzenroth, K. L. Barth, and W. S. Sampath
Materials Engineering Laboratory, Department of Mechanical Engineering
Colorado State University
Fort Collins, CO 80523

ABSTRACT**:** A technology for continuous in-line processing of thin film CdS/CdTe devices has been developed in our laboratory. A CdTe PV device fabrication system has been operating for approximately 6 years and a full prototype manufacturing system for 16.5 x 16.5 inch substrates is under construction. Utilizing this technology, it has been demonstrated that at optimum process conditions good device stability (resistance to performance degradation) can be obtained. Two results pertaining to CdTe device stability are presented here: 1) The process conditions, particularly the $CdCl_2$ treatment, have a significant effect on device stability and 2) a saturation in the loss of efficiency over time in accelerated indoor stress has been observed for a large number of devices.
Keywords: CdTe, degradation, fabrication

1 INTRODUCTION

Since 1991, our work on CdTe PV has led to advances in the areas of: (a) device structure, (b) manufacturing process, and (c) hardware designs suitable for large-scale manufacturing. These advances have been demonstrated on a continuous, in-line process suitable for large volume manufacturing of CdS/CdTe PV devices. This technology has produced devices with an NREL verified efficiency of 12.44 % on unmodified Pilkington TEC 15 substrates [1].

Stability of laboratory CdS/CdTe PV devices has been a matter of concern as shown in a detailed review by Dobson [2]. The stability of CdTe PV devices in commercial production has also been an issue [3]. For these reasons we have placed a considerable emphasis on stability testing and the development of a highly controlled process to produce stable CdS/CdTe devices.

The post deposition $CdCl_2$ treatment [4] is important in the fabrication of CdTe PV devices. It has been found that the $CdCl_2$ treatment has a first order effect on the stability of CdTe PV devices [1,5,6]. A study of $CdCl_2$ treatment with varying processing conditions was performed. It was found that for devices with the same $CdCl_2$ treatment, there is a correlation between the initial current density vs. bias voltage (JV) performance of devices fabricated without the Cu back contact and the stability performance of devices fabricated with the Cu contact application. Better JV performance was correlated to better stability performance. This relationship fits all relevant data for devices processed with the continuous system. The open circuit voltage of cells without the Cu back contact can be used as a quality control metric to predict the stability of as processed devices with the full Cu back contact.

Also in this work it was found that the efficiency of CdTe devices during long term accelerated indoor stress fits a single exponential decay function and that the degradation of performance saturates at long times (in the range of 20,000 ~ 25000 hrs). It was found that for various groups of cells (45 in total) that the saturation efficiency calculated by a curve fit is in the range of 8.5 % ~ 9.5 % .

Exposure of devices to outdoor conditions is also ongoing. When processed at optimal conditions, the devices tested to date maintain good stability under accelerated stress conditions and demonstrate little or no degradation after more than two years of outdoor exposure.

The efficiency of cells in outdoor conditions shows seasonal variations, which make the determination of a trend difficult. It is hoped that in the near future an outdoor degradation rate can be ascertained.

2 CdTe DEVICE FABRICATION

2.1 Fabrication system

The fabrication system is a continuous, all in-line system developed in our laboratory where all device fabrication steps are performed in one vacuum chamber operating at one pressure. An automated conveyor belt extends from air, through all the processing stations in vacuum and then back to air. The cycle time of each process station is 2 minutes, thus one substrate emerges from the system every 2 minutes [1]. Processing steps within the single vacuum boundary include glass heating, CdS and CdTe deposition, $CdCl_2$ heat treatment, back contact formation and back contact heat-treatment. The system operates at 40 mTorr N_2. The required base pressure for the system is only 10^{-4} Torr, allowing the use of low cost hardware. A residual gas analyzer (RGA) is used to monitor chamber gas composition. Process stations are nearly identical in design and construction. This system allows unique processing conditions not available with batch processing to be explored and enables devices to be processed without exposing film interfaces to air. The substrate size for the system is 3.6 x 3.1 inches. The metallization is performed with a low cost spray process using conductive polymers containing C and Ni.

2.2 Larger area processing

We have shown the deposition of CdTe films on 16.5 x 16.5 inch substrates. We are currently constructing a prototype production system for 16.5 x 16.5 inch substrates. This system, if operated for 3 shifts, would have an annual capacity of over 2MW. The pilot 3.6 x 3.1 inch system is a nearly exact simulation of process conditions (substrate temperature, vapor flux and residual gas composition) that will occur on the 16x16 inch substrate system. Thus it is expected that the larger system for processing larger substrates will produce devices with stability, efficiency and yields equal to the current pilot system.

2.3 Device structure

The device structure is glass/SnO_x:F/CdS/CdTe/ carbon coating/nickel coating. The substrates are soda lime glass with the tin oxide coating from Pilkington (TEC 15); the tin oxide is unmodified. These devices have no anti-reflection coating. The back contact is formed in vacuum through the vapor deposition of a copper compound followed by annealing. Metallization, consisting of layers of polymer containing carbon and nickel, is applied by spray processing outside of vacuum. The highest efficiency measured by our laboratory on the devices produced with the pilot system is 13.0%. Several mini-modules of 3.6 x 3.1 inch size have been fabricated. All devices reported in this work have an area of 0.3 cm^2. Fifteen 0.3 cm^2 cells were defined on each 3.1 X 3.6 inch substrate and the glass was cut into 0.5 X 0.75 inch pieces to fabricate 15 separate devices from each substrate. From each substrate groups of 6-9 devices were chosen at random for accelerated stress.

The devices in this work were fabricated with varied $CdCl_2$ treatment. Devices from the same process fabrication run, with the same $CdCl_2$ treatment, were fabricated with and without the application of the Cu containing back contact. The Cu contact was nominally the same in all cases. The metallization for all devices was the same. The JV parameters were measured on both types of devices and fully processed cells with the Cu containing back contact were placed in both indoor accelerated stress and in outdoor conditions.

2.4 $CdCl_2$ treatment

For the devices in this work the $CdCl_2$ treatment was varied, however in all cases it consisted of an exposure of the CdS/CdTe films to a $CdCl_2$ vapor flux for 2 minutes. The substrate temperature was controlled with a heater from the top. In some cases the substrate was held at a higher temperature than the vapor source temperature preventing the deposition of a $CdCl_2$ film. In other cases the source and substrate temperatures were reversed and a $CdCl_2$ film was deposited on the surface of the CdTe layer. The substrate temperature was approximately 512° C on exit from the CdTe deposition step. The substrate temperature dropped to close to 400° C at the end of the $CdCl_2$ vapor exposure step. The ambient gas was dry N_2 with a partial pressure of oxygen in the range of 0.5-1.5%. In all cases after exposure to $CdCl_2$ flux the substrate and films were annealed at ~ 400° C for 2 minutes. In the cases where a $CdCl_2$ film was deposited the film was re-sublimed away from the CdTe surface during this anneal step. The variation of the $CdCl_2$ treatment was part of a process optimization method extending over 2 years and included more than 500 cells.

All processing up to the back contact step was performed in-line and continuously in a single vacuum chamber. There was no wet processing and no chemical etch step before the application of the Cu containing back contact.

3 CORRELATION OF THE $CdCl_2$ TREATMENT AND DEVICE STABILITY

The development of process conditions to produce devices with consistent stability has been the focus of significant effort in our laboratory. The $CdCl_2$ treatment has been found to have a first order effect on eventual device stability. The stability of devices with a copper containing back contact under accelerated stress can be qualitatively predicted using light JV data from devices processed identically without a copper back contact before stress. This relationship fits all relevant data for devices processed with the pilot system. Figure 1 shows the Jsc and Voc of devices fabricated with varied $CdCl_2$ treatment.

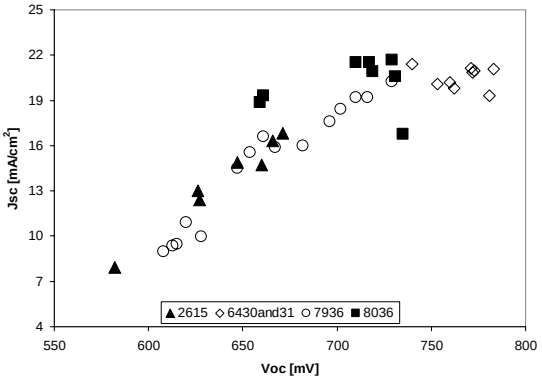

Figure 1: Current density vs. open circuit voltage scatter plot for devices with varied $CdCl_2$ treatment but with no Cu back contact. The insert shows the substrate numbers.

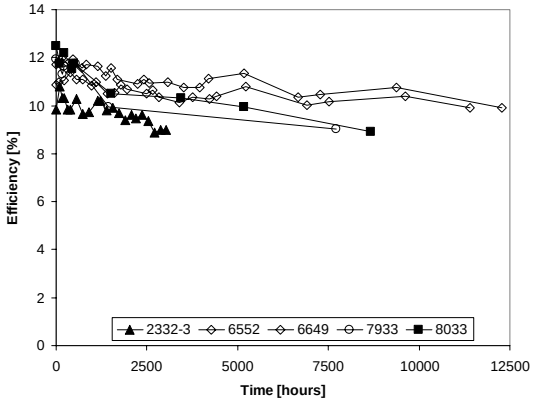

Figure 2: Indoor accelerated stability plot for devices with Cu back contact. Markers for devices with similar $CdCl_2$ treatment are the same in Figure 1 and Figure 2.

Figure 2 shows the average efficiency over accelerated stress time for the same groups of cells as Figure 1, but with the addition of a Cu back contact.

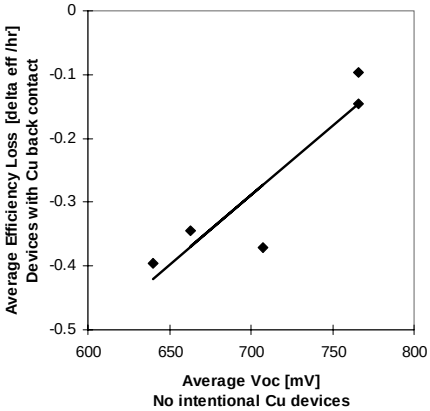

Figure 3: Correlation of device stability to open circuit voltage of devices fabricated without a Cu back contact

There is an obvious correlation between the JV data in Figure 1 and the stability of devices in Figure 2. The use of a single JV parameter allows for a simple quality control metric. Figure 3 shows the correlation of stability to Voc for devices shown in Figures 1 and 2. Higher open circuit voltage leads to better stability. The Voc measurements can be performed directly on the CdTe surface without the need for metallization. A carbon pad and simple digital voltmeter can be utilized. This is a very advantageous quality control metric. This technique could be automated for manufacturing to ensure the production of devices with consistent stability.

4 SATURATION OF EFFICIENCY LOSS DURING LONG TERM ACCELERATED INDOOR STRESS

Some of our devices have been undergoing accelerated stress (lightsoaking) for almost 3.5 years. The stress conditions are: 65° C temperature, cycled (5 hr. on/ 3 hr. off) ~ 1000 W/m^2 illumination, open circuit bias, with a desiccated ambient. The cells are placed in an o-ring sealed enclosure with a temperature controlled water-cooled plate and illumination from quartz halogen lamps. The illumination is cycled on and off by a timer.

Cells are removed periodically from the lightsoak environment and the JV parameters are measured using calibrated ELH lamp illumination. Cells were in groups of 6-9 taken from the same process run and conversion efficiencies are averaged across the group. Cells processed at optimum conditions have shown good stability and the Cu profile as measured by SIMS shows little change due to indoor accelerated stress [2].

For the first ~10,000 hours of lightsoaking the efficiency loss over time appeared to be linear. At the present time groups of cells totaling 45 devices have been undergoing accelerated stress for 20~25,000 total hours and it is apparent that there is a saturation in efficiency which can be fit to a single exponential decay equation of the form:

$$\eta = \alpha \cdot \exp\left(\frac{-t}{\lambda}\right) + \eta_{sat} \qquad [1]$$

Where t is the total time and alpha, lamda, and the saturation efficiency (η_{sat}) are constants determined by the fit. The average efficiency vs. stress time data is shown in Figure 4 along with the calculated line fits.

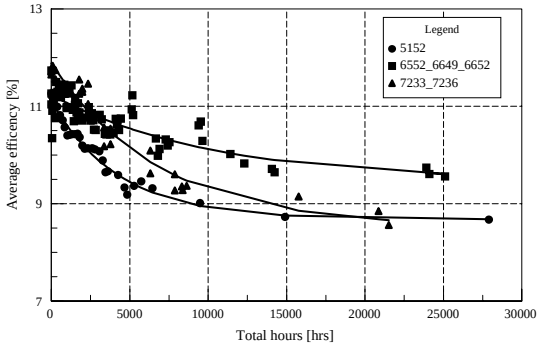

Figure 4: Long term stability plot. Each line represents an average of at least six devices.

The data in Figure 4 was smoothed using a Savatzky-Golay 4th order polynomial routine. The line fit with equation [1] was made using the software Psi Plot 7.5. The line fit correlation parameters ranged from R = 0.86 ~ 0.99 for the fits shown. The line fit for substrates 6552, 6652, and 6649 would require about 60,000 hours of stress to reach the calculated saturation efficiency whereas the line fit for substrate 5152 is saturated at 30,000 hours. The line fits are statistical and no degradation mechanism was assumed.

Table 1 shows the calculated line fit constants including the saturation efficiencies. The percent change in efficiency at saturation as compared to initial efficiency is also included.

Table I: Single exponential decay equation constants

Substrate	α	λ	ηsat [%]	$\Delta\eta$ [% of initial]
5152	2.43	4329	8.7±0.17	-21.9
6552,6652, 6649	1.78	10140	9.5±0.57	-14.3
7233, 7236	3.37	6853	8.5±0.44	-28.3

It has been found that in general open circuit (OC) bias causes the largest changes during accelerated stability testing [7]. It is expected that the $\Delta\eta$ values in Table I would be the worst case. Most stress testing of our devices has been at OC bias conditions. Future work will include stress conditions other than OC bias.

JV parameters for a selected device from substrate 6649 and 7233 devices are given in Table II. As can be seen the main changes in JV parameters are an increase in Roc and a decrease in fill factor. There is also a slight decrease in Jsc but essentially no change in Voc. Analysis of dV/dJ vs. 1/J+JL curves (not shown) presents no evidence of curvature and no indication of the formation of a blocking contact.

Table II: JV parameters of selected devices before and after stress [* stressed 6649-7B: 23908 hr; 7233-2: 20866 hr]

cell	Voc [volts]	Jsc [mA/cm^2]	ff [%]	eff [%]	Roc [ohm cm]
6649-7B	768	20.33	73	11.34	0.87
6649-7B *	763	19.80	63	9.53	2.76
7233-2	729	22.67	69	11.33	0.42
7233-2 *	726	20.44	56	8.37	2.80

5 OUTDOOR STABILITY TESTING

Stability under outdoor conditions continues to be studied.

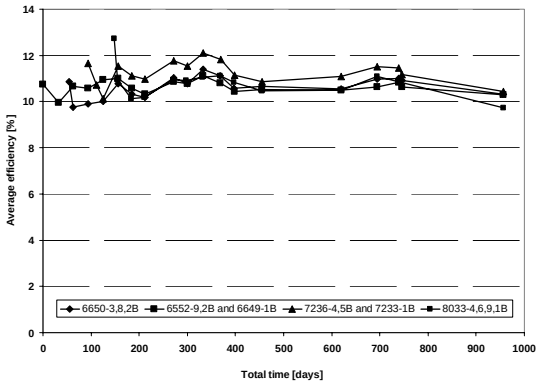

Figure 5: Average outdoor efficiency over time for groups of cells from various process conditions

Enclosed o-ring sealed fixtures, which allow devices to be exposed to the thermal conditions similar to glass on glass encapsulated modules, are utilized [1,3]. The fixtures allow the periodic removal of cells for JV measurement.

Figure 5 shows the latest set of outdoor efficiency vs. time data for 13 cells from 3 different process conditions that are close to the optimum condition. Some devices have been under test for 2.6 years. The test ambient is desiccated with $CaSO_4$ and devices are at OC bias.

There are two peaks in the data at approximately 350 days and 720 days. These peaks are during the summer months. There may be a slight downward trend to the stability plot at times after 300 days. More data will be gathered this summer to check this trend. If a trend is confirmed, a correlation between indoor accelerated stress data presented in section 5 and the outdoor data will be developed using an acceleration factor to modify equation [1]. For the case of OC bias, this will allow the estimation of outdoor life and performance with only one assumption: that the same stability mechanisms apply to indoor accelerated stress and outdoor conditions and only the time scale is changed.

6 CONCLUSIONS

All of the CdS/CdTe devices in this work were fabricated with a continuous in-line system producing 3.1 X 3.6 inch substrates. This process has produced devices with good stability as shown in accelerated indoor stress testing and exposure of devices to outdoor conditions. This process in being scaled to a production prototype for processing 16.5 X 16.5 inch substrates and this system is currently under construction.

A correlation between the $CdCl_2$ treatment and device stability has been established. This shows that the $CdCl_2$ treatment is of significant importance in the fabrication of stable CdTe PV devices. Also measurement of device JV immediately after the $CdCl_2$ treatment (prior to back contact processing) can be used as a quality control metric to predict stability.

Under accelerated lightsoak stress at OC bias and 65° C temperature a large number of cells have shown a saturated leveling in the loss of efficiency over stress time. The total change in efficiency as a percent of initial efficiency was in the range of -14% ~ -28%. Devices fabricated with optimum $CdCl_2$ treatment show better stability under accelerated indoor stress. Since OC bias is generally the most stressful condition, these should be considered lower limit values.

7 ACKNOWLEDGEMENTS

This work is supported by the US National Renewable Energy Laboratory and the US Department of Energy Inventions and Innovation program.

8 REFERENCES:

[1] K. L. Barth, Kurt L., R. A. Enzenroth and W. S. Sampath, "Advances in Continuous, In-Line Processing of Stable CdS/CdTe Devices", 29th IEEE PVSC (2002).

[2] K. D. Dobson, "Stability of CdTe/CdS thin-film solar cells", Solar Energy Materials and Solar Cells, 62 (2000), 295.

[3] T.K. Borg, “Commercial production of thin-film CdTe photovoltaic modules”, NREL/SR-520-23733 National Renewable Energy Laboratory Publication (1997).

[4] B.E. McCandless etal., "Optimization of Vapor Post-deposition Processing for Evaporated CdS/CdTe Solar Cells", Prog. Photovolt. Res. Appl. 7 (1999) 21.

[5] W. S. Sampath etal., "Continuous, in-line processing of stable CdS/CdTe devices", NCPV Program Review Meeting Proceedings (2001).

[6] W. S. Sampath, K. L. Barth and R. A. Enzenroth, "Stability, Yield and Efficiency of CdS/CdTe Devices", NREL Annual Report, Subcontract ADJ-1-30630-07, available at www.engr.colostate.edu/me/facil/mel/.

[7] J. F. Hiltner and J. R. Sites, "Stability of CdTe Solar Cells at Elevated Temperatures: Bias, Temperature, and Cu Dependence", Proceedings NCPV Photovoltaics Program Review (1998) 170.